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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
LAMARRE, GUY J	

ART UNIT	PAPER NUMBER
2133	12

DATE MAILED: 04/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/888,708	PERROT	
	Examiner	Art Unit	
	Guy J. Lamarre, P.E.	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 January 2004* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *7,8,10* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

0. This office action is in response to Applicants' **Amendments** of **24 Jan. 2004**.

0.1 **Claims 13,17** are amended. **Claims 1-32** remain pending.

0.2 The objections and rejections of record are withdrawn in response to Applicants' Amendments.

Response to Arguments

1. Applicants' arguments have been fully considered: they are found persuasive only to the extent that the feature of determining whether input data stream transitions take place in predetermined zone of sample clock is not specifically described by the prior art of record. However **Perigine** (US Patent No. 6,623,185) of IDS of 24 Jan. 2004 teaches such feature in Abstract and in Figs. 1-4.

Claim Rejections - 35 USC ' 103

2. **Claims** 1-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Michel et al. (US Patent No. 6,591,383; 11/19/99) in view of Perigine (US Patent No. 6,623,185).

Referring to claims 1-19 Michel et al substantially discloses "Bit error rate detection", wherein "A method and apparatus for detecting an error rate of a data stream," the data stream is divided into a sequence of blocks, and a detection interval is defined including a predetermined number of blocks in the sequence. For one or more of the blocks in the detection interval, respective error measures are computed responsive to the error rate of the data stream. The one or more blocks in the detection interval are classified as good or bad blocks by comparing the respective error measures to a first threshold. It is estimated that an error condition exists in the data stream by comparing a count of the bad blocks in the interval to a second threshold." (see abstract).

Also, Michel et al. discloses the method including the steps of'... defining a clear interval including a predetermined number of blocks in the sequence; computing the respective error measures for the blocks in the clear interval; classifying the one or more blocks in the clear interval as good or bad blocks by comparing the respective error measures to a third threshold; and estimating that the error condition in the data stream is cleared by comparing a count of the bad blocks in the clear interval threshold to a fourth threshold." (column 3, lines 62-66), "... defining the detection interval includes defining an interval that is no greater than a maximum detection time permitted for estimating that the error condition exists when the error rate of the data stream exceeds a predetermined error level." (column 3, lines 57-60) and method comprising the steps of "... for detecting an error rate of a data stream, including: dividing the data stream into a sequence of blocks; defining a detection interval including a predetermined number of blocks in the sequence; computing for one or more of the blocks in the detection interval respective error measures responsive to the error rate of the data stream; classifying the one or more blocks in the detection interval as good or bad blocks by comparing the respective error measures to a first threshold; and estimating that an error condition exists in the data stream by comparing a count of the bad blocks in the interval to a second threshold." (column 3, lines 6-20). Not specifically described in detail in Michel is the step of determining whether input data stream transitions take place in predetermined zone of sample clock.

However Perigine (US Patent No. 6,623,185) teaches such feature in Abstract and in Figs. 1-4. Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the procedure in Michel by including therein the technique as disclosed by Perigine because such modification would provide the procedure in Michel with a method whereby "counting signal transitions allows detection of abnormal

conditions, such as loss of signals in low-level signals." {See Perigine, Id., col. 10 line 19 et seq.}

3. Claims 1-12 are rejected under 35 U.S.C. 103(x) as being unpatentable over US 5,835,501 to Dalmia et al. in view of Perigine (US Patent No. 6,623,185).

Referring to claim 1, Dalmia et al teaches that "the clocking means is comprised of a voltage controlled oscillator (VCO) for generating a clock signal, and an *A.C.* sine wave signal source *A.C.* coupled to a control input of the VCO for varying the frequency or phase of the clock signal at a predetermined rate." (column 7, lines 40- 45). Also, Dalmia et al teaches that "The test thus is comprised of the steps of generating a jittered clock, using the jittered clock to generate a test data stream, feeding the test data stream to the CRU that is under test, and determining by the BER TESTER 3 the number of bit errors that arise in the CRU's recovered data stream." (column 3, lines 34-39). Dalmia et al. does not explicitly point out to the first time intervals and does not limit the time of intervals, inherently suggesting the possibility to use any intervals including first time interval. Perigine (US Patent No. 6,623,185) teaches such feature in Abstract and in Figs. 1-4.

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use or modify Dalmia by using determination over the plurality of first time intervals whether at least one transition of the data stream occurred in a predetermined phase zone, because one of ordinary skill in the art would use well known principles of the predetermined phase zone (divided zone) in order to provide definition of the bit error rate.

Claims 2-10 depend from respective claim 1, hence inherit the rejection in claim 1. Also, according claims 2-10, Dalmia et al teaches that the "... test determines whether the CRU can correctly recover the data from the data stream that is generated from the specifically jittered clock. The test thus is comprised of the steps of generating a jittered clock, using the jittered

clock to generate a test data stream, feeding the test data stream to the CRU that is under test, and determining by the BER TESTER 3 the number of bit errors that arise in the CRU's recovered data stream. The tolerance or lack of tolerance of the CRU to jitter can be thereby established. ° (column 3, lines 34- 39). Dalmia et al. does not explicitly point out to how many output terminals to use and does not limit the quantity of terminals, inherently suggesting the possibility to use any one or any quantity of terminal including "at least one", and additionally, for example, Lada (US 5,305,323) teaches to use "error counter 165, detector 125 directly counts the number of bit-errors, determined by error detector 110, that occur during a specified measurement (timing) interval. This interval is established by interval counter 205 operating in conjunction with interval selection circuit 250. Upon the occurrence of the first detected error in such an interval, interval counter 205 counts a number of clock pulses up to a preset count established by circuit 250." (column 3, lines 66-68 and column 4, lines 1-3), and "... if the error counter does not attain this count during the interval, both counters 165 and 205 are reset at the end of the interval and await a subsequent occurrence of the next bit-error at which time counters 165 and 205 are restarted to commence the next measurement interval, and so on." (column 4, lines 1419). Perigine (US Patent No. 6,623,185) also teaches such feature in Abstract and in Figs. 1-4.

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use or modify Dalmia by using generating of count value, simplifying a bit error rate indication applicably to the analog signal, providing well known digital-analog conversion, and using the threshold principles for analog signal, because one of ordinary skill in the art would use well known principles of the signal processing to provide the bit error rate detection.

Referring to claims 11, 12, Dalmia et al. teaches that "the clocking means is comprised of a voltage controlled oscillator (VCO) for generating a clock signal, and an A.C. sine wave signal source A.C. coupled to a control input of the VCO for varying the frequency or phase of the clock signal at a predetermined rate." (column 7, lines 4045). Also, Dalmia et al teaches that "The test thus is comprised of the steps of generating a jittered clock, using the jittered clock to generate a test data stream, feeding the test data stream to the CRU that is under test, and determining by the BER TESTER 3 the number of bit errors that arise in the CRU's recovered data stream." (column 3, lines 34-39). Also, Dalmia et al. discloses that "The circuit represents a phase locked loop, which operates in a well known manner at a frequency keyed to the reference clock signal ... " (column 3, lines 61-64), and "The corresponding CRU output (recovered) stream is captured and evaluated using a unit to measure the BER to determine the CRU's jitter tolerance." (column 1, lines 61-64). Also, claim 12 depends from respective claim 11, hence inherit the rejection in claim 11. Dalmia et al. does not explicitly point out to the first time intervals and does not do any limitations, inherently suggesting the possibility to use any intervals including first time interval. Perigine (US Patent No. 6,623,185) also teaches such feature in Abstract and in Figs. 1-4.

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use or modify Dalmia by using determination over the plurality of first time intervals whether at least one transmission of the data stream occurred in a predetermined phase zone, because one of ordinary skill in the art would use well known principles of the predetermined phase zone, evaluation of locking of the phase-locked loop, and comparing signal relatively to a threshold in order to provide definition of the bit error rate.

Claims 13, 14 are similar to claims 1, 4 respectively, and are rejected based on the same rationale thereof.

4. Claim 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5,835,501 to Dalmia et al. in view of Perigine (US Patent No. 6,623,185) in further view of US 5,764,651 to Bullock et al.

Referring to claims 15 Dalmia et al. substantially discloses "means for clocking the data generating means with a jittered clock having a predetermined jitter" (column 7, lines 32,33). Dalmia et al. does not explicitly point out to the "sample clock" but Bullock et al. teaches that "Based on the desired BER detection threshold, the denominator multiple will serve as one component, along with the window length (WL), which determines the data sample period for calculation of the BER." (column 5, lines 60-63). Perigine (US Patent No. 6,623,185) also teaches such feature in Abstract and in Figs. 1-4.

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use or modify Dalmia by using predetermining event of input data stream falling into predetermined portion of sample clock period and error bit rate, because one of ordinary skill in the art would use well known principles of the predetermination of the input data stream "location" and the error bit rate evaluation based on the information about how many of a plurality of evaluation intervals have transitions in the predetermined portion of the sample clock.

5. Claims 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Michel et al. (US Patent No. 6,591,383; 11/19/99) in view of Perigine (US Patent No. 6,623,185) in further view of US 5,835,501 to Dalmia.

According to claims 16-19 Michel et al. teaches to provide "dividing the data stream into a sequence of blocks; defining a detection interval including a predetermined number of blocks in the sequence; computing for one or more of the blocks in the detection interval respective error measures responsive to the error rate of the data stream; classifying the one or more blocks in the detection interval as good or bad blocks by comparing the respective error measures to a first threshold; and estimating that an error condition exists in the data stream by

comparing a count of the bad blocks in the interval to a second threshold." (column 3, lines 6-20). Michel et al. does not explicitly point out to the "sample clock" but Bullock et al. teaches that "Based on the desired BER detection threshold, the denominator multiple will serve as one component, along with the window length (WL), which determines the data sample period for calculation of the BER." (column 5, lines 60-63). Perigine (US Patent No. 6,623,185) also teaches such feature in Abstract and in Figs. 1-4.

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use or modify Michel et al. by teaching Dalmia et al. by using predetermining event of input data stream falling into predetermined portion of sample clock period and error bit rate, generating a count indication and converting the count to the digital value, because one of ordinary skill in the art would use well known principles of the predetermination of the input data stream "location" and the error bit rate evaluation based on the information about how many of a plurality of evaluation intervals have transitions in the predetermined portion of the sample clock.

6. Claims 20-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5,835,501 to Dalmia et al in view of Perigine (US Patent No. 6,623,185).

Referring claim 20, Dalmia et al. substantially teaches that "Jitter is defined in the time domain as the undesirable random, or deterministic time variation of significant events (e.g., rising and/or falling edges) of a digital data stream from a nominal time position. Jitter can be alternatively represented in the frequency domain as undesirable random phase variation of a signal, and hence viewed as phase noise." (column 1, lines 39-45).

Dalmia et al. does not limit the monitoring the indication, inherently suggesting the possibility to use any monitoring including monitoring the indication to determine satisfactory circuit operation or data reception. Perigine (US Patent No. 6,623,185) also teaches such feature in Abstract and in Figs. 1-4. Therefore, it would have been obvious to a person having

ordinary skill in the art at the time the invention was made to modify the procedure in Michel by including therein the technique as disclosed by Perigine because such modification would provide the procedure in Michel with a method whereby "counting signal transitions allows detection of abnormal conditions, such as loss of signals in low-level signals." {See Perigine, Id., col. 10 line 19 et seq.}

According claims 21, 22 Dalmia et al teaches: "As the normal mode of operation of the CSU 1 results from the control input signal to the VCO being a D.C. or very low frequency signal, it has been found to be generally acceptable to add capacitance to the control input without incurring any significant negative performance impact." (column 4, lines 12-16). Dalmia et al. does not limit data rates, inherently suggesting the possibility to use input data stream with varying amounts of jitters. Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use or modify Dalmia by using determination if a bit error occurs according to the plurality of evaluation intervals, because one of ordinary skill in the art would use well known principles of the predetermined phase zone (divided zone) in order to provide definition of the bit error rate.

Referring claim 23 Dalmia et al teaches "the clocking means is comprised of a voltage controlled oscillator (VCO) for generating a clock signal, and an A.C. sine wave signal source A.C. coupled to a control input of the VCO for varying the frequency or phase of the clock signal at a predetermined rate." (column 7, line 40-45). Also, Dalmia et al teaches that "The test thus is comprised of the steps of generating a jittered clock, using the jittered clock to generate a test data stream, feeding the test data stream to the CRU that is under test, and determining by the BER TESTER 3 the number of bit errors that arise in the CRU's recovered data stream. "(column 3, lines34-39), and "clocking means is comprised of a voltage controlled oscillator (VCO) for generating a clock signal, and an A.C. sine wave signal source A.C.

coupled to a control input of the VCO for varying the frequency or phase of the clock signal at a predetermined rate." (column 7, lines 41-45). Dalmia et al. does not limit the possibility of counting provide the indication of number of intervals, inherently suggesting any possibility to use the counter connected to the bit error detect circuit. Perigine (US Patent No. 6,623,185) also teaches such feature in Abstract and in Figs. 1-4.

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use or modify Dalmia by using determination if a bit error occurs according to the predetermined phase zone of a sample and/or evaluation interval, because one of ordinary skill in the art would use well known principles of the predetermined phase zone (divided zone) in order to provide definition of the bit error rate.

6.1 Claims 24-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over US5,835,501 to Dalmia et al. in view of Perigine (US Patent No. 6,623,185) in further view of (US 5,305,323) to Lada.

Dalmia et al substantially discloses "The output of the VCO 7 is connected to an input of a phase detector 8. A reference clock source is connected to the other input of phase detector 8." (column 3, lines 48-50). Dalmia et al. does not explicitly point out to the path, but Lada teaches that "bit-error detector 110 detects bit-errors in a serial bit stream applied via signal path 105 and produces an error pulse, along signal path 120, for each bit error detected. The bit-error detector is conventional and matched to the particular type of serial data stream being monitored." (column 4, lines 20-23). Also, claims 24, 30 depend from respective claim 23, hence inherit the rejection in claim 23.

Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use or modify Dalmia's phase detection by using Lada's paths principles, because one of ordinary skill in the art would use well known principles of the phase error for the input data stream in compliance with IC testing methods.

7. Claims 31, 32 are rejected under 35 U.S.C. 103(x) as being unpatentable over US 5,835,501 to Dalmia et al. in view of Perigine (US Patent No. 6,623,185) in further view of US 5,764,651 to Bullock et al.

Referring to claim 31, Dalmia et al. discloses "means for clocking the data generating means with a jittered clock having a predetermined jitter" (column 7, lines 32,33). Dalmia et al. does not explicitly point out to the "sample clock" but Bullock et al. teaches that "the bit interleave parity contained in frame T for frame T-1 is compared with the calculated value of frame T-1. At step 34, as a result of step 32, the errors which are found between the calculated value and the received value are added to the CUMNUM counter register." (column 6, lines 59-64). Perigine (US Patent No. 6,623,185) also teaches such feature in Abstract and in Figs. 1-4.

Claim 32 depends from respective claim 31, hence inherit the rejection in claim 31. Accordingly, it would have been obvious to one having ordinary skill in the art at the time the invention was made to use or modify Dalmia's sample clock by using Bullock's counter, because one of ordinary skill in the art would use well known principles of the sample clocking with counting and comparison of the evaluation intervals according IC testing methods.

CONCLUSION

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

8.0 Applicant's submission of an information disclosure statement under 37 CFR 1.97(c) with the fee set forth in 37 CFR 1.17(p) on **24 Jan. 2004** prompted the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 609(B)(2)(i). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

3.1 Any response to this action should be mailed to:

Commissioner of Patents and Trademarks, Washington, D.C. 20231

or faxed to: (703) 872-9306 for all formal communications.

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Fourth Floor (Receptionist).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Guy J. Lamarre, P.E., whose telephone number is (703) 305-0755. The examiner can normally be reached on Monday to Friday from 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert De Cady, can be reached on (703) 305-9595.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Information regarding the status of an application may also be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Guy J. Lamarre, P.E
Primary Examiner
4/26/04